REMARKS

At the outset, the Applicants, wish to thank Patent Examiner Thien Tran for the many courtesies extended to the undersigned attorney during the Personal Interview on November 25, 2003, at the U.S.P.T.O. The substance of this Personal Interview is set forth in the Examiner Interview Summary, and in this Amendment.

The amendments to this Patent Application are as follows. The Specification is being amended to correct two minor typographical errors on Page 1 thereof.

The amendments to the claims are as follows. Claims 16-24 directed to process have been cancelled, and have been refiled in a Divisional Patent Application. Newly added claims 25, 26, and 27 are directed to the semiconductor wafer according to the present invention, and are based upon claims 13, 14, and 15 respectively.

The difference between newly added independent claim 25 and previously presented independent claim 13 is that claim 13 recites a semiconductor wafer "comprising", while claim 25 recites a semiconductor wafer "consisting of".

The Patent Examiner has rejected claims 13 - 15 under 35 U.S.C. 103 as being unpatentable over *Wijaranakula et al U.S. Patent No. 6,022,793* in view of *Graef et al U.S. Patent No. 5,935,320.*

The present invention is directed to a semiconductor wafer, comprising a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon;

said substrate wafer having a resistivity of from 0.1 to 50 Ωcm, an oxygen concentration of less than $7.5*10^{17}$ $atcm^{-3}$ and a nitrogen concentration of from $1*10^{13}$ to $5*10^{15}$ $atcm^{-3}$; and

the epitaxial layer has a thickness of from 0.2 to 1.0 µm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 µm can be detected.

Wijaranakula in column 3 in lines 8-25 discloses a method of creating gettering sites in an epitaxial wafer, the method comprising

implanting silicon ions into a substrate of the wafer;

implanting oxygen ions into the substrate of the wafer;

thermally annealing the substrate of the wafer for a period of time sufficient to nucleate defects in the substrate; and

depositing an epitaxial layer upon a surface of the substrate, thereby forming gettering sites from the nucleated

defects in the wafer.

Thus, there is a semiconductive wafer comprising a substrate and an epitaxial layer on the substrate, wherein the substrate contains dislocation loops as gettering sites anchored by oxygen precipitate clusters so as to prevent the dislocation loops from sliding to the surface of the wafer over time.

Wijaranakula in column 6 in lines 7 to 18 discloses that the thickness of the epitaxial layer may be, for example, from less than 1μm up to about 100 μm, preferably from less than 1 μm up to 15μm. The epitaxial layer, like the substrate, may be doped with any suitable dopant including, for example, boron, phosphorous, antimony, arsenic and the like. The dopant concentrations may be similar to those for the substrate discussed above, although the epitaxial layer may contain a lower concentration of dopant than the substrate. The epitaxial layer may also have a specific resistivity similar to that of the substrate, for example ranging from about 5 mΩcm to about 40 Ωcm, preferably 0.1 to 15 Ωcm .

However, *Wijaranakula* fails to disclose doping with nitrogen or providing an epitaxial layer having a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.

Graef in column 2 in lines 40 to 50 discloses a process for producing silicon wafers with low defect density, comprising the steps of:

a) preparing a silicon single crystal having an oxygen doping concentration of at least $4*10^{17}/cm^3$ and a nitrogen doping concentration of at least $1*10^{14}/cm^3$;
b) processing the silicon single crystal to form silicon wafers; and
c) annealing the silicon wafers at a temperature of at least 1000°C, for at least one hour.

However, *Graef* fails to disclose an epitaxial layer with fewer than 30 LLS defects with a size of more than 0.085 µm.

During the Personal Interview, it was pointed out that the present invention distinguishes over *Wijaranakula*, because this reference teaches implanting silicon ions into the substrate wafer. The present invention is devoid of this step; and newly added claim 25 recites "consisting of" so as to clearly exclude any implanted silicon ions.

During the Personal Interview, the Patent Examiner suggested Comparative Testing, and requested an explanation as to the

"surface" on the epitaxial layer to which reference is made.

In response thereto, the undersigned attorney is attaching to this Amendment, an EXHIBIT A, which is a Response to the Patent Examiner's position in which one of the inventors (Dr. Blietz) distinctly points out that the claimed invention has both novelty and nonobviousness in view of the cited prior art. He also provides convincing arguments against a Comparative Testing Program which was requested by the Patent Examiner. Also this patent application is being refiled as an RCE in order to have the Patent Examiner consider all of the Amendments and documents concurrently filed herewith.

In summary, claims 13 to 15 and 25 to 27 are pending, and claims 16 to 24 were cancelled without prejudice. In view of these amendments, it is firmly believed that the present invention, and all the claims, are patentable over all the prior art cited by the Patent Examiner under 35 U.S.C. 103. A prompt notification of allowability is respectfully requested.

Respectfully submitted,

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Enclosures: 1) Copy Petition for a 3 month Extension of Time
2) EXHIBIT A

EXPRESS MAIL NO. **EL 975567426**
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I hereby certify that this correspondence is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10, on the date indicated above and is addressed to the Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Maria Guastella

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